

MEMORY

**CMOS 2M × 32 BIT
HYPER PAGE MODE DRAM MODULE****MB85344C-60/-70****CMOS 2,097,152 × 32 Bit Hyper Page Mode DRAM Module****DESCRIPTION**

The Fujitsu MB85344C is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of sixteen MB814405C devices. The MB85344C is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85344C are the same as the MB814405C which features hyper page mode operation providing extended valid time for data output and higher speed random access of upto 1,024-bit of data within the same row than the fast page mode. For ease of memory expansion, the MB85344C is offered in a 72-pad Single In-line Memory Module package (SIMM).

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	V
Input Voltage	V _{IN}	-0.5 to +7.0	V
Output Voltage	V _{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I _{OUT}	±50	mA
Power Dissipation	P _D	16	W
Storage Temperature	T _{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB85344C-60/MB85344C-70

■ PRODUCT LINE & FEATURES

Parameter		MB85344C-60	MB85344C-70
RAS Access Time		60 ns max.	70 ns max.
Random Cycle Time		104 ns min.	119 ns min.
Address Access Time		30 ns max.	35 ns max.
CAS Access Time		15 ns max.	20 ns max.
Hyper Page Mode Cycle Time		25 ns min.	30 ns min.
Power Dissipation	Operating Mode	2776 mW max.	2464 mW max.
	Hyper Page Mode	2992 mW max.	2512 mW max.
	Standby Mode	176 mW max.	176 mW max.
	Self Refresh Mode	88 mW max.	88 mW max.

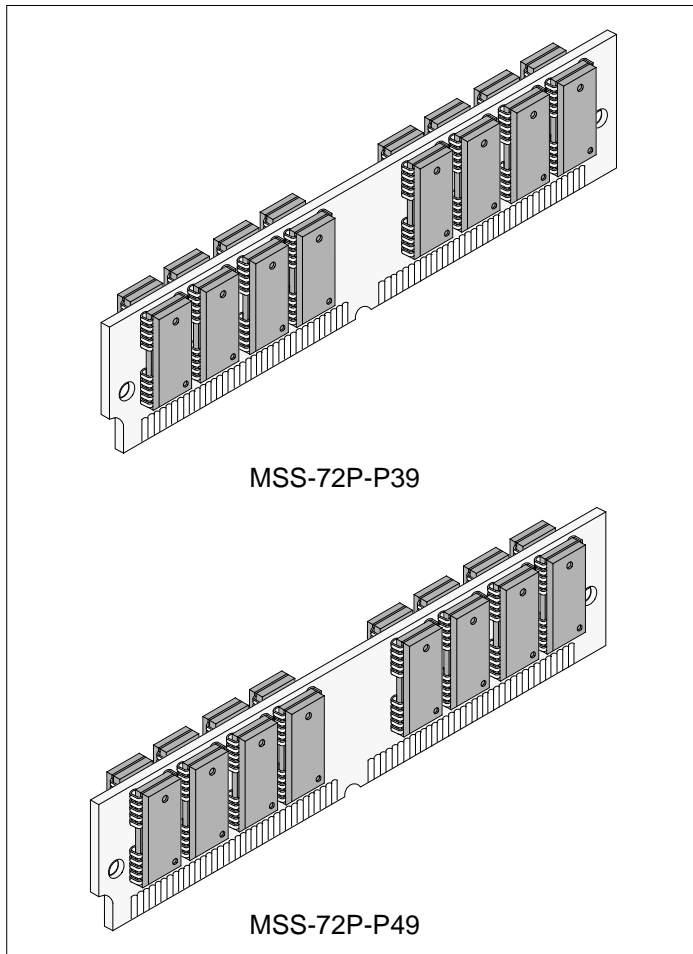
- Organization: 2,097,152 words × 32 bits
- Memory : MB814405C, 16 pcs
- Decoupling Capacitor, 16 pcs
- 5.0 V ± 10% Supply Voltage
- 1,024 Refresh Cycles/16.4 ms
- Hyper page mode operation (EDO)
- Package and Ordering Information:
72-pad SIMM, order as
MB85344C-xxPJPBK
(PJPBK = Gold Pad)
MB85344C-xxPJPB
(PJPB = Solder Pad)

■ PIN ASSIGNMENT

DQ0	2	1	VSS
DQ1	4	3	DQ16
DQ2	6	5	DQ17
DQ3	8	7	DQ18
VCC	10	9	DQ19
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
DQ4	20	19	NC
DQ5	22	21	DQ20
DQ6	24	23	DQ21
DQ7	26	25	DQ22
A7	28	27	DQ23
VCC	30	29	NC
A9	32	31	A8
RAS2	34	33	RAS3
NC	36	35	NC
NC	38	37	NC
CAS0	40	39	VSS
CAS3	42	41	CAS2
RAS0	44	43	CAS1
NC	46	45	RAS1
NC	48	47	WE
DQ24	50	49	DQ8
DQ25	52	51	DQ9
DQ26	54	53	DQ10
DQ27	56	55	DQ11
DQ28	58	57	DQ12
DQ29	60	59	VCC
DQ30	62	61	DQ13
DQ31	64	63	DQ14
NC	66	65	DQ15
PD2	68	67	PD1
PD4	70	69	PD3
VSS	72	71	NC

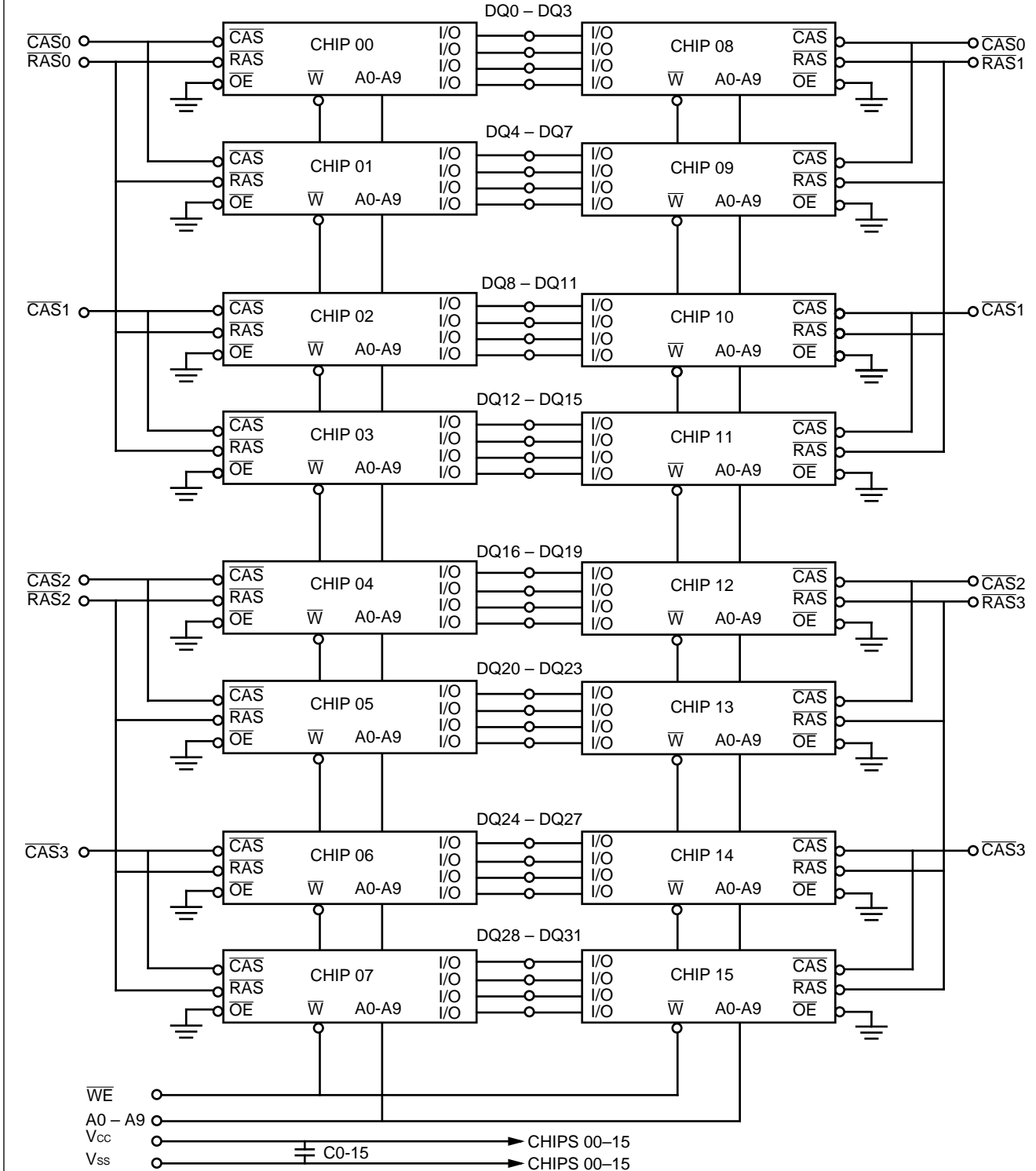
Pin #	Symbol	-60	-70
67	PD1	NC	NC
68	PD2	NC	NC
69	PD3	NC	Vss
70	PD4	NC	NC

■ PACKAGE



MB85344C-60/MB85344C-70

FUNCTIONAL BLOCK DIAGRAM



MB85344C-60/MB85344C-70

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, all inputs*	V_{IL}	-0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

Note: *Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min.	Max.	Unit	
Output High Voltage*1	$I_{OH} = -5 \text{ mA}$	V_{OH}	2.4	—	V	
Output Low Voltage*1	$I_{OL} = 4.2 \text{ mA}$	V_{OL}	—	0.4	V	
Input Leakage Current	\overline{RAS}	$I_{I(L)}$	-30	30	μA	
	\overline{CAS}					
	Address, \overline{WE}					
0 V $\leq V_{IN} \leq 5.5 \text{ V}$, 4.5 V $\leq V_{CC} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, all other pins not under test = 0 V						
Output Leakage Current	0 V $\leq V_{OUT} \leq 5.5 \text{ V}$, Data out disabled	$I_{O(L)}$	-10	10	μA	
Operating Current*2 (Average power supply current)	MB85344C-60	\overline{RAS} & \overline{CAS} cycling, $t_{RC} = \text{min.}$	I_{CC1}	—	504	mA
	MB85344C-70			—	448	
Standby Current (Power supply current)	TTL Level	$\overline{RAS} = \overline{CAS} = V_{IH}$	I_{CC2}	—	32	mA
	CMOS Level	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$		—	16	
Refresh Current #1*2 (Average power supply current)	MB85344C-60	$\overline{CAS} = V_{IH}$, $\overline{RAS} = \text{cycling}$, $t_{RC} = \text{min.}$	I_{CC3}	—	504	mA
	MB85344C-70			—	448	
Hyper Page Mode Current*2	MB85344C-60	$\overline{RAS} = V_{IL}$, $\overline{CAS} = \text{cycling}$, $t_{HPC} = \text{min.}$	I_{CC4}	—	544	mA
	MB85344C-70			—	456	
Refresh Current #2*2 (Average power supply current)	MB85344C-60	$\overline{RAS} = \text{cycling}$, \overline{CAS} -before- \overline{RAS} , $t_{RC} = \text{min.}$	I_{CC5}	—	408	mA
	MB85344C-70			—	368	
Refresh Current #3 (Average power supply current)	MB85344C-60	$\overline{RAS} = \overline{CAS} \leq 0.2 \text{ V}$, Self refresh	I_{CC9}	—	16	mA
	MB85344C-70			—	16	

Notes: *1. Referenced to V_{SS} .

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$, $V_{IL} > -0.3 \text{ V}$.

I_{CC1} , I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.

I_{CC4} is specified at one time of address change during one Page cycle.

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■ CAPACITANCE

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A0 to A9	C_{IN1}	—	88	pF
Input Capacitance, $\overline{RAS0}$ and $\overline{RAS3}$	C_{IN2}	—	34	pF
Input Capacitance, $\overline{CAS0}$ to $\overline{CAS3}$	C_{IN3}	—	30	pF
Input Capacitance, \overline{WE}	C_{IN4}	—	85	pF
I/O Capacitance, (DQ0-DQ31)	C_{DQ}	—	15	pF

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■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85344C-60		MB85344C-70		Unit	Notes
			Min.	Max.	Min.	Max.		
1	Time Between Refresh	t _{REF}	—	16.4	—	16.4	ms	
2	Random Read/Write Cycle Time	t _{RC}	104	—	119	—	ns	
3	Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	ns	4, 7
4	Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	ns	5, 7
5	Column Address Access Time	t _{AA}	—	30	—	35	ns	6, 7
6	Output Hold Time	t _{OH}	5	—	5	—	ns	
7	Output Hold Time from $\overline{\text{CAS}}$	t _{OHc}	5	—	5	—	ns	
8	Output Buffer Turn On Delay Time	t _{ON}	0	—	0	—	ns	
9	Output Buffer Turn Off Delay Time	t _{OFF}	—	15	—	15	ns	8
10	Output Buffer Turn Off Delay Time from $\overline{\text{RAS}}$	t _{OFFR}	—	15	—	15	ns	8
11	Transition Time	t _T	1	50	1	50	ns	
12	$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	45	—	ns	
13	$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	100000	70	100000	ns	
14	$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	ns	
15	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	0	—	0	—	ns	
16	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	14	45	14	50	ns	9, 10
17	$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	10	10000	10	10000	ns	
18	$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40	—	50	—	ns	
19	$\overline{\text{CAS}}$ Precharge Time (Normal)	t _{CPN}	10	—	10	—	ns	15
20	Row Address Setup Time	t _{ASR}	0	—	0	—	ns	
21	Row Address Hold Time	t _{RAH}	10	—	10	—	ns	
22	Column Address Setup Time	t _{ASC}	0	—	0	—	ns	
23	Column Address Hold Time	t _{CAH}	10	—	10	—	ns	
24	$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	12	30	12	35	ns	11
25	Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	ns	
26	Column Address to $\overline{\text{CAS}}$ Lead Time	t _{CAL}	23	—	28	—	ns	
27	Read Command Setup Time	t _{RCS}	0	—	0	—	ns	
28	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	ns	12
29	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0	—	0	—	ns	12
30	Write Command Setup Time	t _{WCS}	0	—	0	—	ns	13

(Continued)

MB85344C-60/MB85344C-70

■ AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85344C-60		MB85344C-70		Unit	Notes
			Min.	Max.	Min.	Max.		
31	Write Command Hold Time	t _{WCH}	10	—	10	—	ns	
32	\overline{WE} Pulse Width	t _{WP}	10	—	10	—	ns	
33	Write Command to \overline{RAS} Lead Time	t _{RWL}	15	—	18	—	ns	
34	Write Command to \overline{CAS} Lead Time	t _{CWL}	10	—	10	—	ns	
35	DIN Setup Time	t _{DS}	0	—	0	—	ns	
36	DIN Hold Time	t _{DH}	10	—	10	—	ns	
37	Data Hold Time from \overline{RAS}	t _{DHR}	50	—	55	—	ns	
38	\overline{RAS} Precharge Time to \overline{CAS} Active Time (Refresh Cycles)	t _{RPC}	5	—	5	—	ns	
39	\overline{CAS} Setup Time (C-B-R Refresh)	t _{CSR}	0	—	0	—	ns	
40	\overline{CAS} Hold Time (C-B-R Refresh)	t _{CHR}	10	—	10	—	ns	
41	\overline{WE} Setup Time from \overline{RAS}	t _{WSR}	0	—	0	—	ns	17
42	\overline{WE} Hold Time from \overline{RAS}	t _{WHR}	10	—	10	—	ns	17
43	DIN to \overline{CAS} Delay Time	t _{DZC}	0	—	0	—	ns	
44	\overline{WE} to Data In Delay Time	t _{WED}	15	—	15	—	ns	
45	\overline{RAS} to Data In Delay Time	t _{RDD}	15	—	15	—	ns	
46	\overline{CAS} to Data in Delay Time	t _{CDD}	15	—	15	—	ns	
47	\overline{RAS} to Column Address Hold Time	t _{AR}	26	—	26	—	ns	
48	Write Command Hold time Referenced to \overline{RAS}	t _{WCR}	24	—	24	—	ns	
49	Data Input Hold Time Referenced to \overline{RAS}	t _{DHR}	24	—	24	—	ns	
50	Hyper Page Mode \overline{RAS} Pulse Width	t _{RASP}	—	200000	—	200000	ns	
51	Hyper Page Mode Read/Write Cycle Time	t _{HPC}	25	—	30	—	ns	
52	Access Time from \overline{CAS} Precharge	t _{CPA}	—	35	—	40	ns	7, 14
53	Hyper Page Mode \overline{CAS} Precharge Time	t _{CP}	10	—	10	—	ns	
54	Hyper Page Mode \overline{RAS} Hold Time from \overline{CAS} Precharge	t _{RHCP}	35	—	40	—	ns	
55	\overline{RAS} Pulse Width for Self Refresh	t _{RASS}	100	—	100	—	ns	16
56	\overline{RAS} Precharge Time for Self Refresh	t _{RPS}	104	—	119	—	ns	16
57	\overline{CAS} Hold time for Self refresh	t _{CHS}	-50	—	-50	—	ns	16

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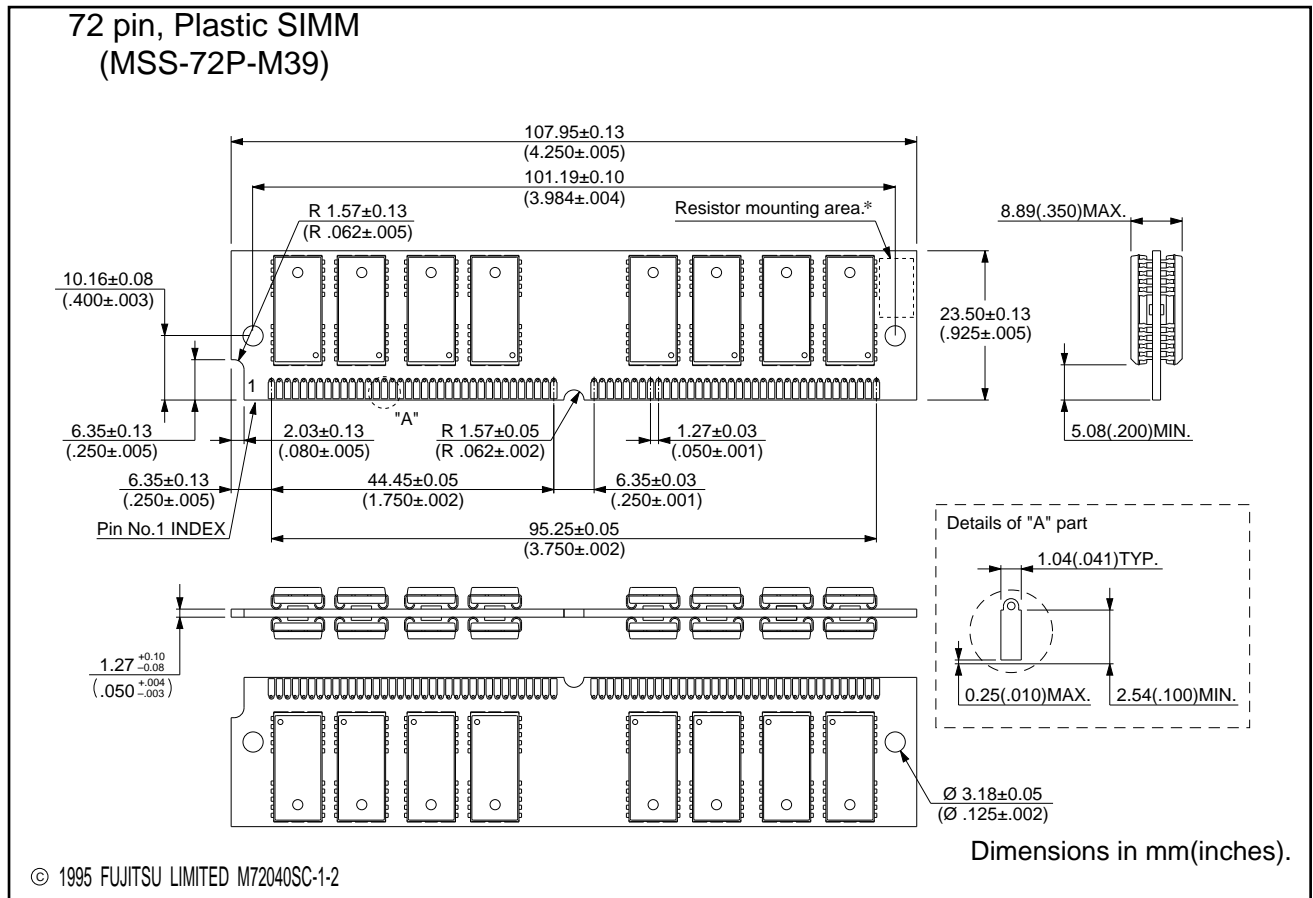
- Notes: 1. An initial pause ($\overline{RAS}=\overline{CAS}=V_{IH}$) of $200\mu s$ is required after power-up followed by any eight \overline{RAS} -only cycles or eight \overline{CAS} -before- \overline{RAS} refresh cycles ($\overline{WE}=V_{IH}$) before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight \overline{CAS} -before- \overline{RAS} initialization cycles are required instead of eight \overline{RAS} cycles.
2. AC characteristics assume $t_T = 2$ ns.
 3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
 4. Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$, $t_{RAD} \leq t_{RAD}(\text{max.})$. If t_{RCD} and/or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
 5. If $t_{RCD} \geq t_{RCD}(\text{max.})$, $t_{RAD} \geq t_{RAD}(\text{max.})$, and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC} .
 6. If $t_{RAD} \geq t_{RAD}(\text{max.})$ and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
 7. Measured with a load equivalent to two TTL loads and 100 pF.
 8. t_{OFF} and t_{OFR} are specified that output buffer change to high impedance state.
 9. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 10. $t_{RCD}(\text{min.}) = t_{RAH}(\text{min.}) + 2 t_T + t_{ASC}(\text{min.})$.
 11. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}(\text{min.})$ the data output pin will remain High-Z state through entire cycle.
 14. t_{CPA} is access time from the selection of a new column address (caused by changing \overline{CAS} from "L" to "H"). Therefore, if t_{CP} become long, t_{CPA} also become longer than $t_{CPA}(\text{max.})$.
 15. Assumes that \overline{CAS} -before- \overline{RAS} refresh cycle.
 16. Assumes that \overline{CAS} -before- \overline{RAS} self refresh cycle.
 17. Assumes test mode function.

*Source: See MB814405C Data Sheet for details on the electricals.

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■ PACKAGE DIMENSIONS

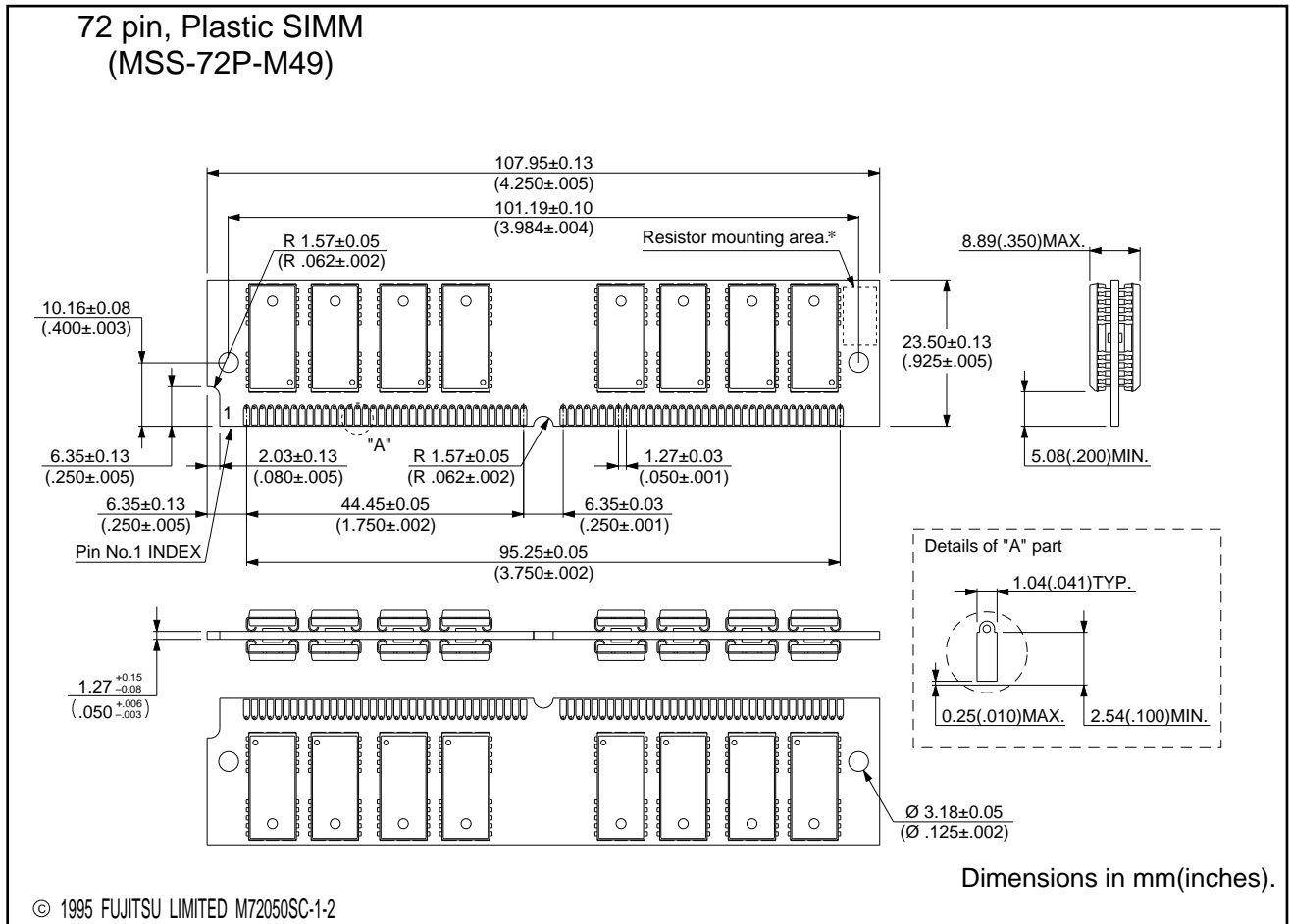
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■ PACKAGE DIMENSIONS

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